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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,006	06/20/2003	Koji Hosono		5769

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HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/601,006	HOSONO ET AL.
	Examiner	Art Unit
	Gene N Auduong	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-17* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06-20-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on June 20, 2003 is being considered by the examiner.

Claim Objections

3. Claims 10-17 are objected to because of the following informalities: Claims 10, 12-14 and 15 seem to be an independent claim (a memory card or an electronic device) that depending on another independent claim (a specific memory circuit). Appropriate correction is required.

4. Claims 11, 16 and 17 are objected to as being dependent upon the objected base claims 10, 14 and 15, respectively.

5. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten into independent claim including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-4 and 6-17 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamamoto et al. (U.S. Pat. No. 6,438,035).

Regarding claim 1, Yamamoto et al. disclose a nonvolatile semiconductor memory device (figures 1 and 5) comprising: a memory cell array 1 in which electrically rewritable floating gate type memory cells MC are arranged; and a plurality of sense amplifier circuits (sense amplifiers section 8) configured to read data from the memory cell array 1, wherein each of the sense amplifier circuit (in sense amplifier section 8) configured to sense cell data of a first memory selected from the memory cell array 1 under a read condition determined in correspondence with cell data of a second memory cell RMC adjacent to the first memory cell and written after the first memory cell (col. 8, lines 2+; col. 12, lines 42+).

Regarding claim 2, Yamamoto et al. disclose the non-volatile semiconductor memory device according to claim 1, wherein each the sense amplifier circuit (sense amplifier circuits in sense amplifier section 8) comprises a first latch circuit LA for holding a read data of the first memory cell MC; a second latch circuit RLA for holding a data read out from the second memory cell RMC prior to data read of the first memory cell as a reference data; a first sense node (sense node sen0 – sen3) connected to a bit line BL of the memory cell array 1 via a clamping transistor (pull-up/pull-down transistors) used for clamping and amplifying bit line BL potential; a second sense node to which the first and second latch circuits are commonly connected through the respective transfer gates (transfer gate TR); first and second data transfer circuits disposed in parallel between the first and second sense nodes, the first and second data transfer circuits being switch in response to the reference data held in the second latch circuit to selectively transfer one of cell data of the first memory cell under first and second read

conditions to the first latch circuit (data transfer circuits being switch in response to the reference data held in the second latch circuit RLA; figure 5).

Regarding claim 3, Yamamoto et al. disclose the non-volatile semiconductor memory device according to claim 2, wherein the first and second read condition are determined by changing a read voltage applied to the first memory cell (col. 8, lines 13+).

Regarding claim 4, Yamamoto et al. disclose the non-volatile semiconductor memory device according to claim 2, wherein the first and second read condition are determined as corresponding to differences of bit line discharge times determined due to the first memory cell (col. 8, lines 13+).

Regarding claim 6, Yamamoto et al. disclose the non-volatile semiconductor memory device according to claim 2, wherein each of the sense amplifier circuit further comprises: a first precharge transistor (pull-up transistor) connected to the first sense node for precharging a selected bit line of the memory cell array 1; and a second precharge transistor connected to the second sense node for precharging second node (figure 5).

Regarding claims 7-9, Yamamoto et al. disclose the non-volatile semiconductor memory device according to claim 1, wherein the memory cell array comprises a plurality of NAND cell units arranged therein, each NAND cell unit having a serial circuit of a plurality of memory cells, a first select gate transistor disposed between one end of the serial circuit and a bit line, and a second select gate transistor disposed the other end of the serial circuit and a common source line, each of the memory cell having a floating gate a control gate stack thereabove; wherein the control gate of the memory cells in each of the NAND cell unit are connected to different word lines (each of the word lines connecting each of the memory cell in its rows), respectively, and

wherein the gate of the first and second select gate transistors in each of the NAND cell unit are connected to select gate lines, respectively; and wherein a plurality of memory cells arranged along a word line and connected to different bit line, respectively, constitute a page which serve as a unit for parallel data read and parallel data write, and wherein the plurality of sense amplifier circuits constitute a page buffer for sensing data of one page (figure 5, col. 12, lines 42+; figure 11, col. 1, lines 21+).

Regarding claims 10-17, a memory device as claimed in claim 1 can be formed in a memory card that can used in any electric device or built directly into the electronic device for storing data, such as digital camera, an audio player, etc. Inherently, such device would have interface circuit and card slot for connecting and controller for accessing and storing the data in the memory card.

Allowable Subject Matter

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not show or fairly suggest, in addition to other element in the claim, claiming the structure and function for the circuit as claimed; claiming the non-volatile semiconductor memory device having the first data transfer circuit comprise first and second transistors serially disposed between the first and second sense nodes, the first transistor being gate controlled by a first data node of the second latch circuit, the second transistor being driven by a first sense-use control signal to turn-on, and wherein the second data transfer circuit comprise third and fourth transistors serially disposed between the first and second sense nodes, the third transistor being gate controlled by a second data node of the second latch circuit, the fourth transistor being driven by a second sense-use control signal to turn-on, the second sense-

use control signal being generated at a timing different from that of the first sense-use control signal.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
July 03, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818